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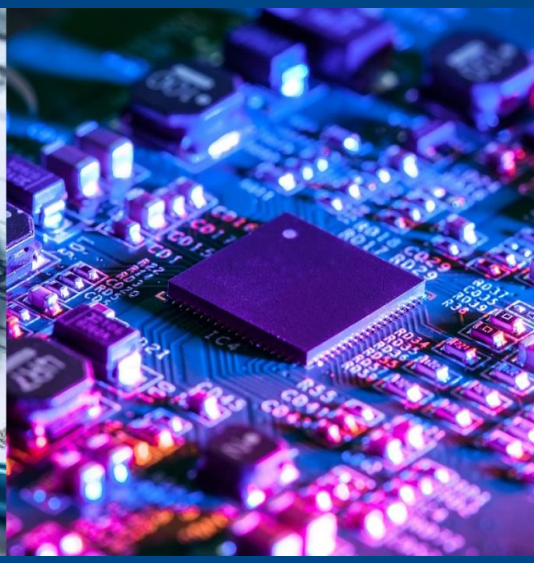

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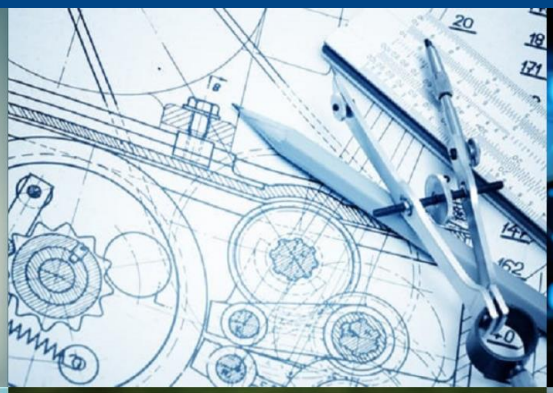

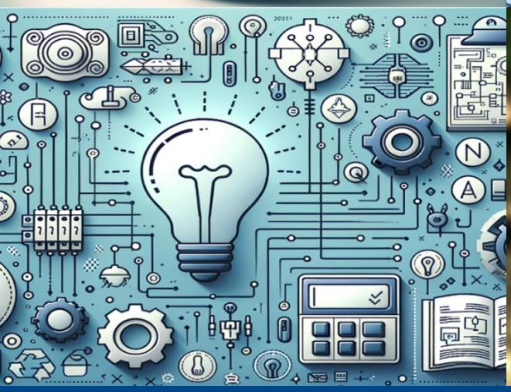

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Design and Optimize the Performance-area Trade-off Parallel-Prefix Adder

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ABSTRACT: Two operand additions are indispensable operations in almost every embedded system and DSPs (Digital Signal Processors). It is also considered as a basic requisite for other arithmetic operations. However, there is always a trade-off among the speed, area and power dissipation of adders that determines the overall performance of the system. In the addition operation, the carry propagation being one of the performance issues, puts a limit on its speed.In this project, we focus on synthesizing approximate parallel-prefix adders using the Split-Accuracy Configuration method. This method divides the operands into two parts to minimize carry-propagation delay, leading to higher throughput, lower latency, and faster addition.

KEYWORDS: Approximate Adders, Parallel Prefix Adders, Area-Efficient, Split-Accuracy

I.INTRODUCTION

Approximate computing explores a new way of allowing minimizing hardware components to compute possibly inaccurate results with goal of saving area, as well as power consumption [1].The design of approximate adders is not a pretty task to implement but open up a new space of more designs[2].It is not always true that a hardware component is capable of replacing selected transistors from specific blocks[3].But Approximation can implemented in the arithmetic operations by removing certain gates or flip-flops from a desired part in the given netlist[4].

In this work, we focus on the design of approximate parallel-prefix adders. As we are on the digital world era, every operation that is performed by machines, computers, electronic items is of the form binary bits only. So Arithmetic Operations play a major role in performing tasks or instructions.Out of a wide range of adder organizations, parallel-prefix adders are capable of saving area and power that are more efficient and versatile and can meet multiple design criteria and constraints. Parallel Prefix can model multiple adder forms spanning from ripple carry adders (RCAs) ,Carry increment adders and fast adders of logarithmic logic depth as well as everything in between[5]

Our aim is to optimize the performance and area trade-off of approximate parallel prefix adders . In this project, we will use split accuracy configuration in order to minimize the carry propagation length. In split accuracy configuration we will configure LSB 8 bits with approximation of designing carry propagation and upper MSB 8 bits with standard Approximation adder structures (i.e. Kogge Stone, Brent-Kung, Ladner-Fischer, Sklansky, Han-Carlson Adders)

A. Parallel Prefix Addition Calculation and Formula

When adding two n-bit binary numbers X =Xn−1, Xn−2, . . . , X0 and Y = Yn−1, Yn−2, . . . , Y0, the sum bit Si at the i^{th} bit position is computed by combining the modulo-2 sum (XOR) of bits Xi and Yi, i.e., Hi = Xi ⊕Yi (XOR), and the carry Ci−1 computed in the previous bit position [1]

$$Si = Hi \oplus Ci-1. \quad (1)$$

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For computing the sum bits of the following bit positions, the incoming carry Ci−1 needs to propagate to the next position. The carry out of the ith bit position Ci is computed using the local carry generate and propagate bits Gi = Ai . Bi (AND)and Pi = Ai + Bi (OR) and the fundamental recursive carry propagation formula [1]

$$C_i = G_i + P_i C_{i-1} \quad (2)$$

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B. Accurate Parallel Prefix Adder

Mapping carry-look ahead adders to parallel-prefix structures maximizes their efficiency and increases their placement and

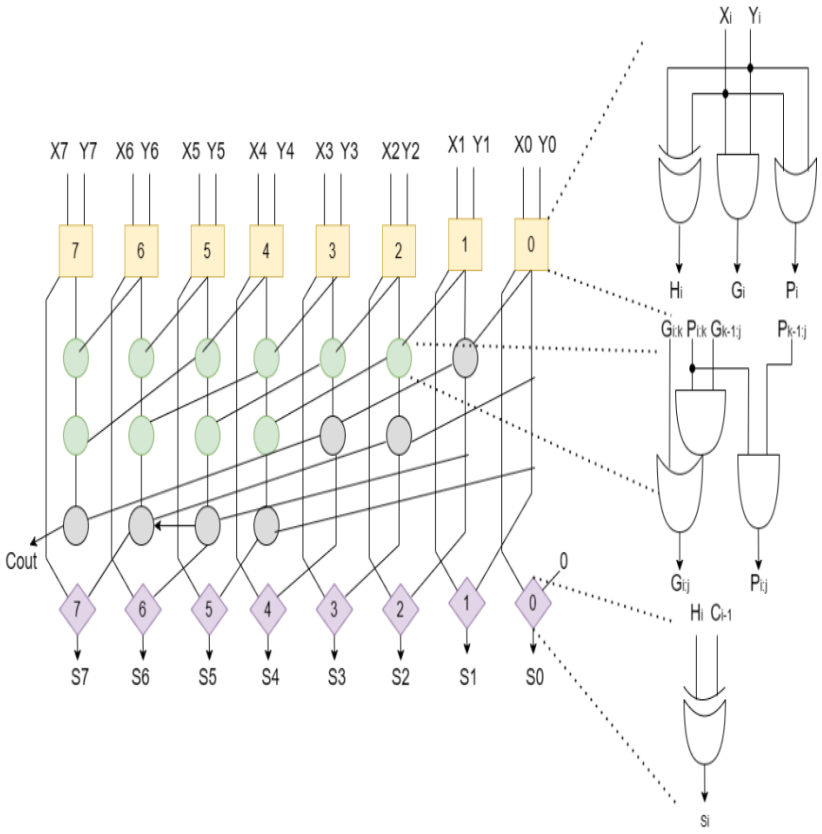

Figure 1-Kogge Stone Adder

wiring regularity [5] [6] [7].Carry computation is trans- formed to a prefix problem by using the associative operator ◦ which associates pairs of generate and propagate bits as follows:

$$(G, P) \circ (G', P') = (G + P G', P P'). \quad (3)$$

In a series of consecutive associations of generate and propagate pairs, (Gk:j , Pk:j) denotes the group generate and prop-agate term produced out of bits k, k − 1, . . . , j

$$(G_{k:j}, P_{k:j}) = (G_k, P_k) \circ (G_{k-1}, P_{k-1}) \circ \cdots \circ (G_j, P_j) \quad (4)$$

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II.LITERATURE REVIEW

Before coming to the methodology, let us review about literature from different reference papers for getting better clarity:

1. Apostolos Stafanidis, Ioanna Zoumpouli dou et al[1]: This paper introduces AxPPAs, a PPA approximation based on estimations taken from Pos. Each of these uses less energy than the others. Examine the effectiveness of the AxPPA-LF in light of recent improvements in energy-saving devices. When applied to available data on energy quality and area quality, the AxAs framework reveals the existence of a fresh Pareto front.

2. M. Pashaeifar, M. Kamal, A. Afzali-Kusha and M. Pedram et al[2]: In this paper, we focus on the synthesis of approximate parallel-prefix adders. Instead of exploring specific architectures, as done by state-of- the-art approaches, the introduced synthesizer can produce every solution that meets the designer's criteria, resulting in adders with various delay, area, and error trade-offs. This automatic design space exploration allows approaching in several cases, optimal solutions that could have not been designed with any other known parallel-prefix architecture.

3. Gupta, D. Mohapatra, A. Raghunathan and K. Roy et al[3]: In this paper, we studied a reinforcement learning(RL) Based approach to designing parallel prefix circuits such as adders or priority encoders that are functional to high-performance digital design. Unlike prior methods, our approach designs solutions tabula rasa purely through learning with synthesis in the loop. We design a grid-based state-action representation and an RL environment for constructing legal prefix circuits.

4. Schlachter, V. Camus, K. V. Palem and C. Enz et al[4]: This paper analysis in detail the state of the parallel prefix adder architectures and provide new designs that minimizes power consumption and critical path delays. The speed and area efficiency benefits of the parallel prefix designs with through simulations and comparison is reviewed. This research have ramifications for high performance computing systems and point to interesting avenues to further the sate of the art in parallel prefix adder design.

5. R. Zimmermann et al[5]: The paper explores binary adder architectures optimized for cell-based VLSI (Very Large-Scale Integration) design, covering their implementation, performance, and synthesis methodologies.it analysis of various adder topologies (e.g., ripple-carry, carry-lookahead, carry-select, etc.).It shows optimization strategies for speed, area, and power in CMOS-based designs. This will automated synthesis techniques for generating efficient adder circuits in standard-cell environments.

6. S. Roy, M. Choudhury, R. Puri and D . Z . Pan et al[6]: This paper mainly focuses on Optimizes parallel-prefix adders (e.g., Brent-Kung, Kogge-Stone, Han-Carlson) for performance-area trade-offs in VLSI design , Balances logic depth (delay) and wire length (area/power)..This paper gives the uses graph-based optimization to explore prefix structures.It demonstrates improved delay-area trade-offs compared to traditional fixed-topology adders

In the conclusion, the parallel prefix adder using split accuracy configuration with approximation i.e. on LSB side and on MSB side, implementing the structure with high precision Ladner Fischer Approximate Parallel Prefix Adder which gives us better delay and less area. This method takes time due to approximation part on the LSB side in which we have do trial and error method for each approximation structure made. The main reason to do approximation on the LSB side is ,if there is a sudden change on the LSB value in compare to the orginal value then it doesn't shows a huge difference because the main application of our proposed method is in Image processing. In Image Processing each pixel of the imagehas a RGB color code which is in hexa decimal value. So We can say that our proposed method is mainly focus on the Image processing only

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III.METHODOLOGY

The Methodology block diagram consists of steps as shown below:

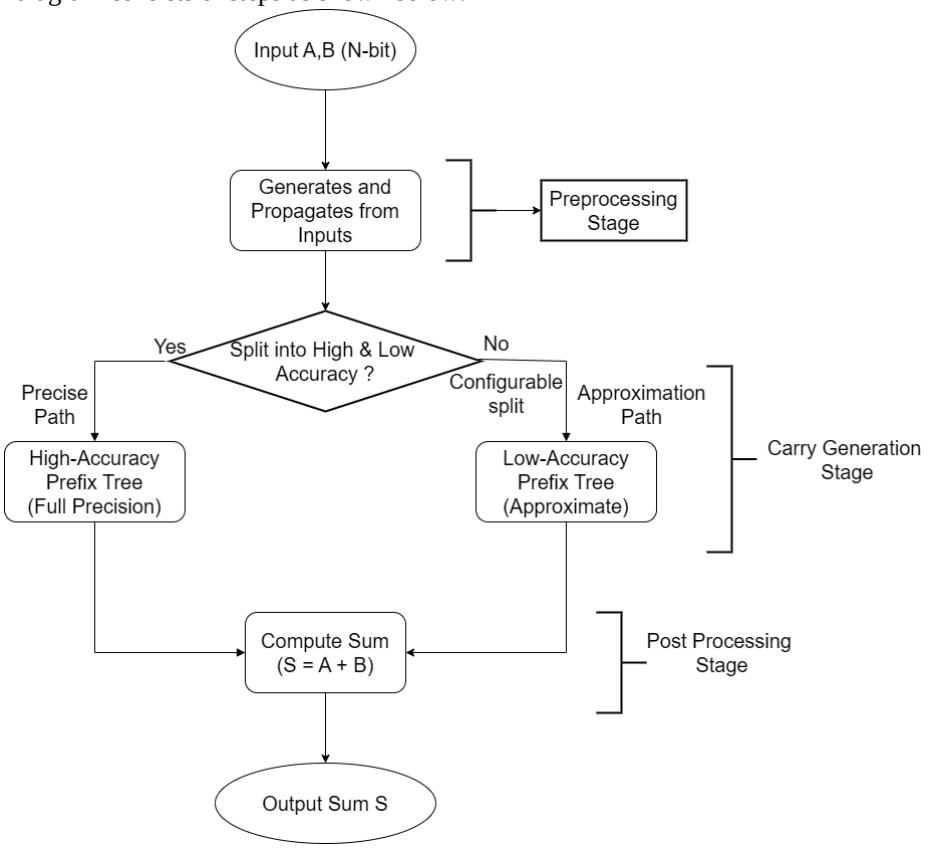

Figure 2-Work Flow Diagram

From the above workflow there consist mainly 3 stages

1. Pre Processing Stage
2. Carry Generation Stage
3. Post Processing Stage

1.Pre Processing Stage: As we can see from the above Workflow Diagram, we will consider two binary bits A, B of size N. From the two binary bits A,B , let us generate Generates and Propagates of the Carry. In Approximation Structure consists of different blocks and each block represents a structure of different gates.

2.Carry Generation: Carry Generation Stage is the important stage in the parallel prefix adder in order to minimize the Carry Propagation Length , minimizing the Hardware and delay with it. There is a series of levels or stages which carry will generate or propagate from one bit position to another bit position. Here in this stage we would like to apply Split Accuracy Configuration and divide the whole N bits into N/2 bits. Selecting one N/2 bits into the High Accuracy part which gives a Full Precise Value that almost matches with the original value. Coming to the other part, N/2 bits into the Low Accuracy part which gives an approximate value that may or may not match with the original value.

3.Post Processing Stage: Post Processing Stage is the final stage in order to do parallel prefix computation which results in obtaining Sum and Carry, i.e., output addition of two binary bits
The architecture of Approximate Parallel Prefix adder gives the less delay for the operation of 16-bit addition. The properties of the operations are evaluated in parallel and accept the trees to overlap which leads to parallelization. When minimum carry-chain length is close to the adder's bit width, only a very small amount (if any) of operations can

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be saved. In Fig. 3, the number of operators reduces when dropping the requirement of minimum carry-chain length below 12 bits. The second observation is that for carry-chain lengths of 8 bits (half the total bit width of the adder) or less, the maximum fan-out constraint is not critical any more, since all results converge to the same number of operators. This is expected since, as the minimum carry chain required is lowered, less operators will belong to the same chain, and there are less

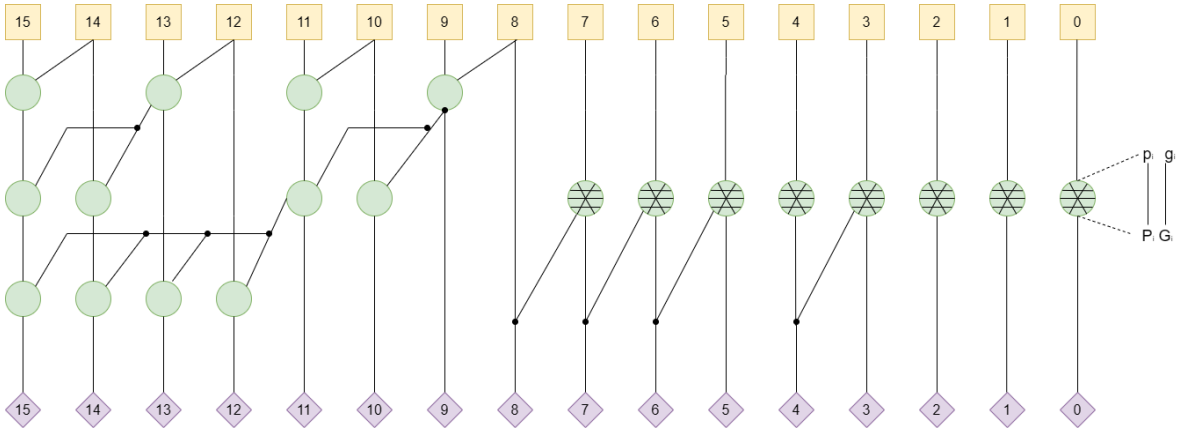

Figure 3 – Approx Structure

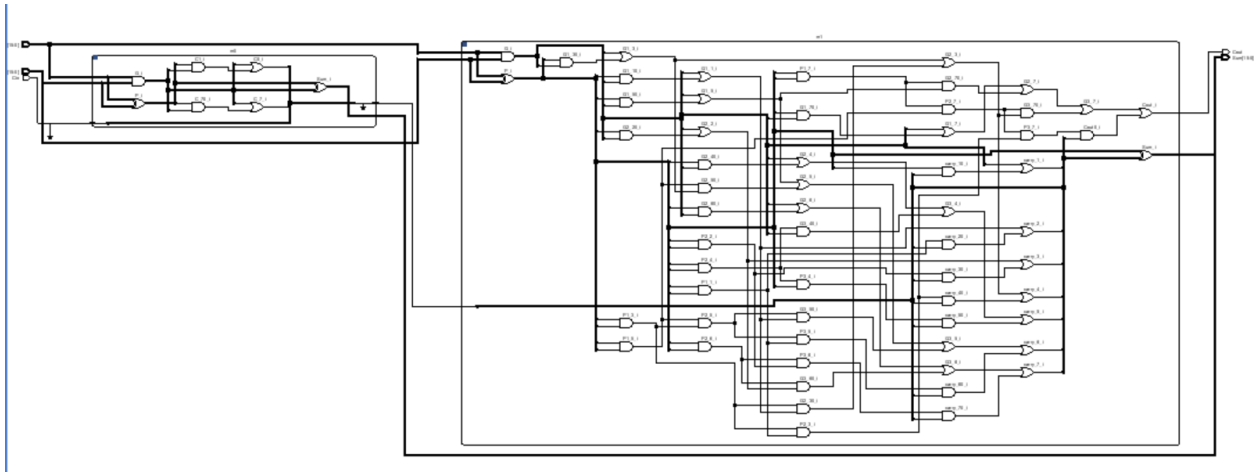

Figure 4-Block Diagram generated from the verilog code

opportunities for an operator to reach its maximum fan-out constraint. In overall, as the accuracy constraint is relaxed, the maximum fan-out constraint becomes increasingly less important, and eventually for extremely relaxed cases, this does not impact the result at all.

IV.RESULTS AND COMPARISION

After doing simulations with numerous inputs we have compare the total no of gates that are used in our method and existed method. Below table shows some of the results

Parameter	Existed Method	Proposed Method
Total no.of Gates Used	108	93
Delay(Approx)	11.48(ns)	11.29(ns)
EF	0.32	0.33

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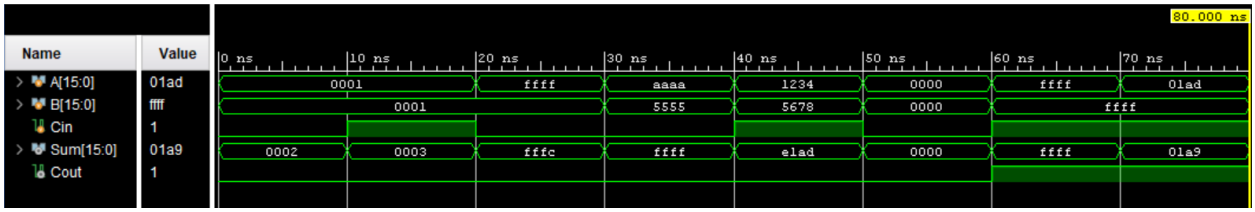
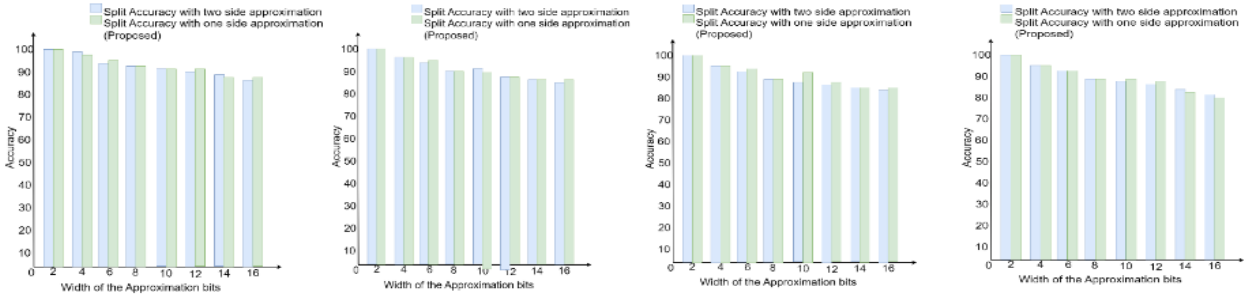


Figure 5 – Simulation Results



(a)15 Input Samples **(b) 30 Input Samples** **(c) 50 Input Samples** **(d) 100 Input Samples**

Figure 6 -Accuracy Rate for different input samples

V.CONCLUSION AND FUTURE WORK

In this paper, a new approach to design an efficient 16 bit Approximate Parallel Prefix concentrates on gate levels to improve the speed and decreases the area. It is like tree structure and cells in the carry generation stage are decreased to speed up the binary addition. The proposed adder addition operation offers great advantage in reducing delay.

REFERENCES

[1] Apostolos Stefanidis,Ioanna Zoumpoulidou,Dionysios Filippas,Giorgos Dimi trakopoulos,Georgios Ch. Sirakoulis "Synthesis of Approximate Parallel-Prefix Adders" IEEE Transactions on Very Large Scale Integrations (VLSI) systems, Vol. 31,no . 11, November 2023.

[2] M. Pashaeifar, M. Kamal, A. Afzali-Kusha, and M. Pedram, "A the- oretical framework for quality estimation and optimization of DSP applications using low-power approximate adders," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 66, no. 1, pp. 327–340,Jan. 2019.

[3] V. Gupta, D. Mohapatra, A. Raghunathan, and K. Roy, "Low-power digital signal processing using approximate adders," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 32, no. 1, pp. 124–137, Jan. 2013.

[4] J. Schlachter, V. Camus, K. V. Palem, and C. Enz, "Design and applications of approximate circuits by gate-level pruning," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 25, no. 5, pp. 1694–1702, May 2017.

[5] R. Zimmermann, "Binary adder architectures for cell-based VLSI and their synthesis," Ph.D. dissertation, Swiss Federal Inst. Technol. (ETH) Z¨urich, Z¨urich, Switzerland,1998.

[6] S. Roy, M. Choudhury, R. Puri, and D. Z. Pan, "Towards optimal performance-area trade-off in adders by synthesis of parallel prefix structures," in Proc. 50th ACM/EDAC/IEEE Design Autom. Conf. (DAC), May 2013, pp. 1–8.

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